Search Notes

Application/Control No.	Applicant(s)/Patent under Reexamination	
10/724,011	HEER, CHRISTOPH	
Examiner	**Art Unit**	
Peter Coughlan	2129	

SEARCHED

Class	Subclass	Date	Examiner
706	1	6/10/2006	PDC
706	15	6/10/2006	PDC
706	45	6/10/2006	PDC
700	1	6/10/2006	PDC
700	90	6/10/2006	PDC
365	185.2	6/10/2006	PDC
358	1.9	6/10/2006	PDC
711	108	6/10/2006	PDC
703	17	6/10/2006	PDC
364	200	6/10/2006	PDC
716	5	6/10/2006	PDC
326	46	6/10/2006	PDC

INTERFERENCE SEARCHED

Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)

	DATE	EXMR
East--d flip flops, node, input output, if then else, LUT, comparison, MUX multiplexer, CLB, configurable logic blocks	6/10/2006	PDC
East--II--look up table, logic control, register, input control node, schematic, switch, bus, comparator, event dectector,	6/10/2006	PDC
East--III--xilinx, infineon,	6/10/2006	PDC
Inventor Christoph Heer	6/10/2006	PDC
IEEE--Christoph Heer, circuit 'if then else' d flip flop, LUT look up table, CLB configurable logic block, , schematic	6/10/2006	PDC
Dogpile--Christoph Heer, circuit 'if then else' d flip flop, LUT look up table, CLB configurable logic block, , schematic	6/10/2006	PDC
365/185.2 with switching circuit, input 711.108 with 'if then else', address bus, comparand register, comparator circuits	**6/10/2006**	**PDC**
703.17 with FPGA chip, bus, DMA engine	6/10/2006	PDC